REMARKS

This application has been carefully reviewed in light of the final Office Action dated April 19, 2006. Claims 1 to 4 and 7 to 9 are pending in the application, with Claims 5 and 6 having been cancelled. Claim 1, the sole independent claim, has been amended. Reconsideration and further examination are respectfully requested.

In the Office Action, Claims 1 to 9 were rejected under 35 U.S.C. § 102(e) over U.S. Patent No. 6,347,294 (Booker); and Claim 4 was rejected under 35 U.S.C. § 103(a) over Booker in view of U.S. Patent No. 6,041,400 (Ozcelik). Reconsideration and withdrawal are respectfully requested.

Referring specifically to the claims, independent Claim 1 as amended is directed to a processor system on a single semiconductor substrate. The processor system is provided with a built-in processor, a memory controller, an external bus interface that can connect an external processor from outside of a single semiconductor substrate, a processor bus which is connected with the built-in processor and the external bus interface, and a connection unit that mutually connects the memory controller and the processor bus. The built-in processor and the external bus interface are responsive to respective enable signals. One of the respective enable signals is asserted while the other one of the respective enable signals is deasserted, so that one of the built-in processor and the external bus interface corresponding to the asserted enable signal can be used exclusively.

Thus, among its many features, the present invention provides that a built-in processor and an external bus interface are responsive to respective enable signals, and that one of the respective enable signals is asserted while the other one of

the respective enable signals is deasserted, so that one of the built-in processor and the external bus interface corresponding to the asserted enable signal can be used exclusively. The applied references of Booker and Ozcelik are not seen to disclose or suggest at least this feature.

As understood by Applicants, Booker discloses that an EXCPU 14 and an EMCPU 26 obtain common access to a DCRX logic 160. The EXCPU 14 gains control of DCRX logic 160 or memory interface through arbitration. See Booker, column 5, line 57 to column 6, line 5; and Figure 4.

However, nothing in Booker is seen to disclose or suggest that a built-in processor and an external bus interface are responsive to respective enable signals, muchless that one of the respective enable signals is asserted while the other one of the respective enable signals is deasserted, so that one of the built-in processor and the external bus interface corresponding to the asserted enable signal can be used exclusively.

Ozcelik has been reviewed and is not seen to compensate for the deficiencies of Booker. In particular, although column 6, lines 40 to 42 and Figure 3 of Ozcelik may be seen to disclose that a media processor circuit arrangement 60 includes a plurality of processing cores 62, Ozcelik is not seen to disclose or suggest that a built-in processor and an external bus interface are responsive to respective enable signals, and that one of the respective enable signals is asserted while the other one of the respective enable signals is deasserted, so that one of the built-in processor and the external bus interface corresponding to the asserted enable signal can be used exclusively.

Accordingly, based on the foregoing amendments and remarks, independent Claim 1 as amended is believed to be allowable over the applied references.

The other claims in the application are each dependent from the independent claims and are believed to be allowable over the applied references for at least the same reasons. Because each dependent claim is deemed to define an additional aspect of the invention, however, the individual consideration of each on its own merits is respectfully requested.

No other matters being raised, it is believed that the entire application is fully in condition for allowance, and such action is courteously solicited.

Applicant's undersigned attorney may be reached in our Costa Mesa, California office at (714) 540-8700. All correspondence should continue to be directed to our below-listed address.

Respectfully submitted,

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